Estimating the gate-source voltage inside the device

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Abstract

In recent years, next-generation semiconductors have been gaining attention in power electronics equipment, with GaN being particularly anticipated for the miniaturization of power converters driven by high frequencies. However, the gate withstand voltage of GaN is approximately 6V, and there is a concern that voltage oscillations during switching could lead to dielectric breakdown. This study proposes a method to model the gate voltage oscillations within the device, including parasitic components of the package and wiring, during the device's ON state, Measurements indicated that the gate voltage oscillated beyond the withstand voltage due to the significant influence of source inductance. However, the model suggested that the internal gate oscillations were smaller and within the withstand voltage range.

1. Introduction

In recent years, as the effects of climate change have become more pronounced, environmental considerations have been gaining increasing importance. In response, efforts toward carbon neutrality have been accelerating worldwide, and in Japan, the Green Growth Strategy associated with achieving carbon neutrality by 2050 has been announced(1). The advancement of power electronics technology is expected to play a significant role in achieving carbon neutrality, and the widespread adoption of next-generation semiconductors such as SiC and GaN will greatly contribute to the proliferation of power electronics devices and energy conservation(2)(3). These next-generation semiconductors exhibit superior physical properties, such as bandgap and breakdown electric field, compared to conventional Si semiconductors. In particular, GaN semiconductors are known to adopt a high-electron-mobility transistor (HEMT) structure, allowing the use of the two-dimensional electron gas formed at the AlGaN/GaN interface as a current path(4). This enables a reduction in input capacitance for devices with the same ON resistance, leading to expectations for the miniaturization and efficiency improvement of power converters through high-frequency operation(5).

In a power converter, power control is performed by switching the power device ON and OFF. When in the ON state, it is necessary to sufficiently reduce the on-resistance of the current path to minimize losses. To achieve this, an overdrive is used, in which a voltage large enough to secure the current path is applied between the gate and source. For GaN devices, a voltage of at least 4.5 V is required for overdrive. However, the gate withstand voltage is relatively low at approximately 6 V, resulting in a small margin between the applied voltage and the withstand voltage(6). Consequently, there is little tolerance for the gate-source withstand voltage, raising concerns that voltage surges and subsequent oscillations due to high-speed switching could easily exceed the withstand voltage and cause device failure. To address this issue, semiconductor manufacturers are working on defining instantaneous gate withstand voltage ratings(7) and developing GaN devices with higher gate withstand voltages(8).

Additionally, the device's chip is packaged in a resin mold for protection against foreign objects, making it impossible to directly measure the voltage between the gate and source. While the voltage at the electrode terminals on the exterior of the package can be measured, it is affected by parasitic components between the chip and the electrode terminals, making it difficult to obtain an accurate voltage reading.

In this study, we propose a method for estimating the voltage oscillation applied to the gate-source capacitance inside a device by modeling the turn-on behavior of the device in a half-bridge circuit, which is commonly used in power converters, taking into account parasitic components in the wiring and within the device package.

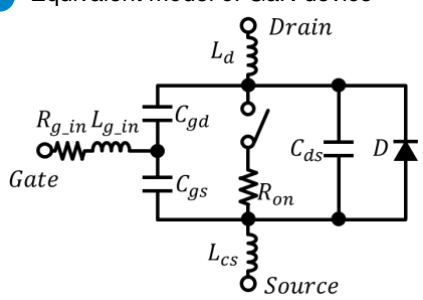
2. Circuit Modeling During Turn-On

In this study, we model the switching behavior during the turn-on operation of the Lo side device in a half-bridge circuit.

2.1. Parasitic Components of Power Semiconductor Devices

The equivalent model of a GaN device is represented as

Figure 1 Equivalent model of GaN device



shown in Figure 1. In general, the gate voltage refers to the voltage across the gate-source capacitance, Cgs. However, as mentioned earlier, actual measurements inevitably include the effects of factors such as the common source inductance, Lcs, inside the package, as well as the resistance and inductance of the wiring. As a result, accurately measuring the voltage of Cgs is challenging.

2.2 Model Construction

Figure 2 illustrates an equivalent circuit of an ideal half-bridge circuit that includes parasitic components of semiconductor devices and the wiring board on which the devices are mounted. To account for the DC current flowing during turn-on, an L-load is connected between the drain and source of the Hi side switch. The DC current is reflected in the model by setting an initial value for the L-load current during calculations. When the Lo side switch turns ON, the Hi side switch is OFF while the Lo side switch is ON. Consequently, the AC current flows through the path via the inter-terminal capacitance on the Hi side, the channel resistance on the Lo side, and the bypass capacitor Csnb. The DC current flows from the power supply through the L load.

Figure 2 Equivalent circuit that includes parasitic components

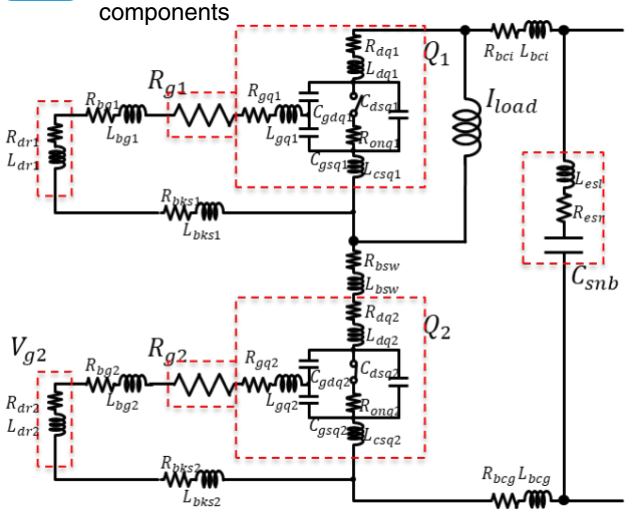
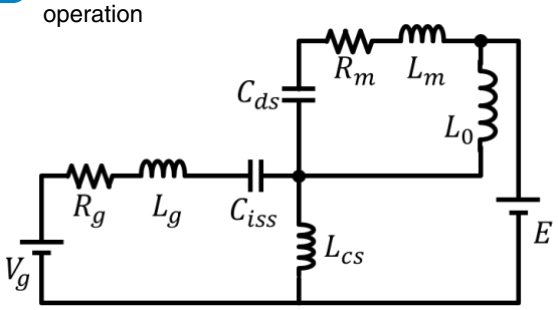


Figure 3 shows a simplified model for representing gate voltage oscillations. Since the Lo side transistor Q2 is in the ON state, its channel resistance is small and can be considered negligible. In this case, the gate-source capacitance Cgs is expressed as the input capacitance Ciss, which includes the feedback capacitance Cgd. In this model, the voltage

Figure 3 Simplified model of Lo side device during turn-on operation



applied to Ciss is defined as the gate voltage. For the Hi side transistor Q1, when considering the composite capacitance among its drain, source, and gate terminals, the drain-source capacitance Cds is dominant and is therefore reflected in the model. The resistance and inductance components present in the alternating current path are represented as Rm and Lm, respectively. Furthermore, the resistance and inductance components in the Lo side gate drive circuit are denoted as Rg and Lg, respectively, and the voltage applied between the gate and source is represented as Vg. The resistive and inductive components present in the Hi side gate drive circuit do not affect its behavior during turn-on and are therefore omitted in this model.

Since the bypass capacitor Csnb is sufficiently large compared to Cds, it can be considered a power supply in the AC path. At the same time, it can also serve as the power supply in the DC path, and in this model, it is treated as power supply E.

3. Evaluation and Verification

3.1. Determination of Parameters and Initial Conditions

To verify the validity of this model, the values of device and Wiring Board parameters were substituted into each parameter of the simplified model to calculate the voltage waveform. Table 1 presents a list of parameters used for the voltage waveform calculation.

The operating conditions were set with a power supply voltage of 100 V and an initial current of 12 A flowing through the inductive load. To simulate switching behavior, at time t = 0, the model's electrical state was changed by applying step responses to both the power supply voltage E (0 → 100 V) and the Lo side gate voltage Vg (0 → 5.2V), and the voltage waveform was calculated.

The GaN device used was the EPC2010C. Considering the voltage applied to both the Hi side and Lo side devices immediately before turn-on, the Ciss value was taken from the datasheet at approximately 0 V, while the Cds value was taken at 100 V(7). A common source inductance, Lcs, of 300 pH was used (9). To compare with the actual device data discussed later, the resistance and inductance components of the Wiring Board were analyzed using ANSYS Q3D Extractor based on the Wiring Board design data, and the corresponding parameters were extracted.

Table 1 List of parameters

Symbol	Parameter	Symbol	Parameter
Rm	0.5 Ω	Ciss	420 pF
Lm	7.8 nH	Cds	240 pF
Rg	11.5 Ω	Lcs	300 pH
Lg	19.8 nH	L_0	174 uH
E	0 → 100 V	Vg	0 → 5.2 V

3.2. Verification of Model Validity

To evaluate the validity of the voltage oscillation model, a comparative assessment with actual equipment was conducted using double-pulse evaluation. To measure the gate voltage, a probing terminal was placed as close to the device as possible, and an optically isolated probe (TIVP05, manufactured by Tektronix) was used. A comparison between the measured waveform and the modeled waveform is shown in Figure 4. The dashed line represents the measured waveform, while the solid line represents the modeled waveform. In the comparison waveform shown in Figure 4, the time when the turn-on begins and current starts flowing through the Lo side channel is set as 0 seconds. In this model, transient changes in the device have not been considered, so the waveforms do not overlap. However, the waveform shapes and oscillation frequencies match with high accuracy. Specifically, the oscillation frequency of the modeled waveform is 114.9 MHz, while that of the measured waveform is 117.9 MHz, resulting in an error of 2.5 percent.

When comparing the peak values of the gate voltage, the peak value of the modeled waveform was 8.51 V, while the peak value of the measured waveform was 7.42 V, resulting in an error of 12.8 percent. This discrepancy is likely because, in the modeled waveform, E and Vg were given a step response to simulate switching behavior. Consequently, the change was steeper than the measured waveform, leading to the observed difference in the peak gate voltage.

3.3. Estimation of Internal Gate Voltage of Device

Using this model, we estimate the actual gate voltage inside the device (Ciss voltage in this model). Figure 5 shows the voltage waveform of Ciss calculated under the same conditions using the model. As seen in Figure 5, the oscillation of the Ciss voltage is smaller than the voltage that includes Lcs, which can actually be measured. The peak voltage is 5.80 V, which falls within the withstand voltage range. This indicates that the reverse electromotive force generated in the inductance due to the change in current during turn-on has a significant effect. The magnitude of the generated reverse electromotive force V is expressed using the change in drain current dId/dt in equation (i).

$$V = L_{cs} * \frac{dI_d}{dt} \quad \cdots\cdots\cdots\cdots (i)$$

Although Lcs is as small as 300 pH, the current in GaN changes on the order of several nanoseconds. As a result, the change in drain current is large, leading to a significant induced electromotive force. Consequently, there is likely a considerable discrepancy between the measured voltage waveform and the actual gate voltage inside the device. A significant drop in gate voltage immediately after switching begins is also considered to be influenced by Lcs. The waveform estimated from the model suggests that the peak gate voltage inside the device is lower than the measured value and does not exhibit large voltage oscillations as seen in the measurements. Therefore, even for devices with low gate withstand voltage, such as GaN, it can be assumed that they operate without issues. As a result, it becomes possible to further increase the switching speed or apply a higher gate voltage, thereby reducing switching losses.

Figure 4 Comparison of measured waveform and modeled waveform

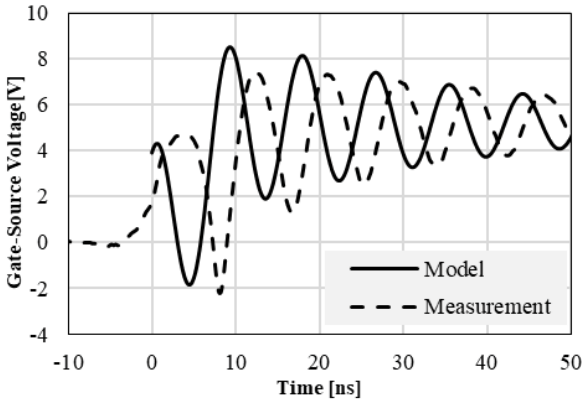


Figure 5 Voltage waveform of internal gate voltage of device calculated using the model

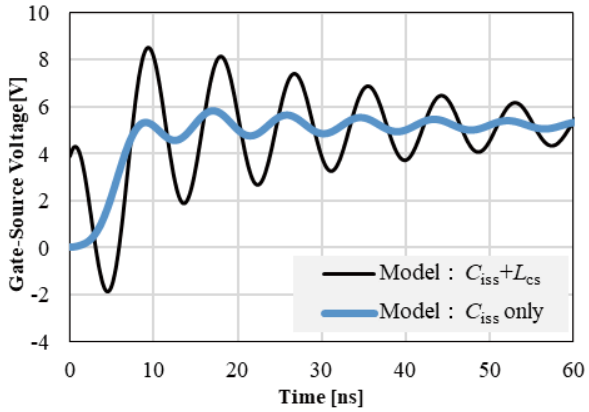


Figure 6 Peak value mapping of gate voltage when Lm and Lg are varied

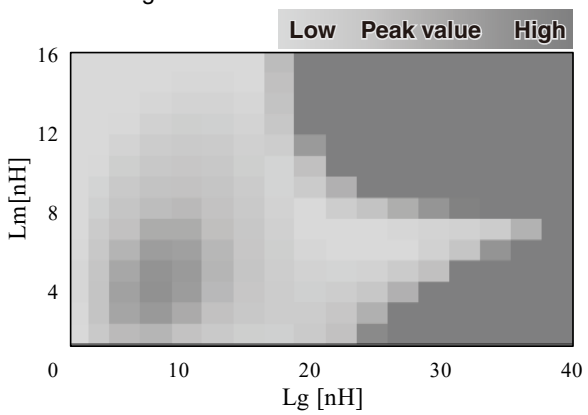


Figure 6 presents a peak value mapping of the gate voltage when the two inductances, Lm and Lg, in the model are varied parametrically. In general, inductance in switching circuits is required to be minimized. However, as shown in Figure 6, simply reducing the inductance does not necessarily minimize the peak value. By designing the two values in a well-balanced manner, it becomes possible to suppress the peak value of gate voltage oscillation during turn-on.

4. Conclusion

In this study, a circuit model for the turn-on operation of a half-bridge circuit, a common switching circuit, was developed by taking into account the parasitic components included in the device package and the Wiring Board. By using this model, we demonstrated a method for estimating the internal behavior of a device that is difficult to measure in practice. When switching with GaN, the gate withstand voltage is low, making it susceptible to dielectric breakdown due to surges at turn-on and subsequent oscillations. With high-speed switching, when there is a significant change in current, the back electromotive force of the common source inductance causes a substantial difference between the measured waveform and the gate voltage inside the device. However, by using this model to estimate the internal gate voltage of the device, it becomes possible to determine whether the voltage exceeds the withstand voltage. This enables the miniaturization and efficiency improvement of power electronics equipment, making full use of GaN's characteristics of high-speed switching and low loss.

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